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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,021	WHITTAKER STEWART, MARK ANDREW	
	Examiner	Art Unit	
	JUVENA LOO	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10, 13, 15-17, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster et al. (US 2002/0181395 A1) in view of Dell et al. (US 2002/0085578 A1) and further in view of Karp (5,469,154).

Foster et al. discloses a technique for communicating data through a network comprising the following features:

Regarding claim 1, *a connection controller* (Foster: see Figure 3, Network Manager, 370) *for a network comprising a plurality of first stage switches, a plurality of second stage switches coupled to each of the plurality of first stage switches* (Foster: see Figure 1, Interconnect Fabric 110), *and a plurality of packet sources coupled to the plurality of first stage switches* (Foster: see Figure 1, Node 1 through Node N, 105) *and configured to request a traffic pattern for a packet* (Foster: see "The routine receives...executing application" in page 11, section 0093; see also "as part of

registering…destination node" in page 12, section 0097), *the connection controller comprising*:

a network topology cache (Foster: see Figure 9, 903) *capable of being coupled to the network and configured to receive network topology data from the network* (Foster: see Figure 9);

a packing algorithm circuit coupled to the network topology cache (Foster: see Figure 7 and see "FIG. 7 is a…appropriate information" in page 11, section 0093) *and capable of being coupled to the plurality of packet sources* (Foster: see "The routine receives…executing application" in page 11, section 0093), *the packing algorithm circuit configured to:*

receive the network topology data from the network topology cache (Foster: see "If it is instead determined…translation table" in page 11, section 0094),

compute an actual traffic pattern for the packet based on the received network topology data and all the received traffic pattern requests (Foster: see "The routine begins…local destination by using the routing information from the corresponding entry in the virtual identifier translation table" in page 11, sections 0094 and 0095; see also "as part of registering…destination node" in page 12, section 0097; see also "the network manager…with the configuration information" in page 13, section 104), *and*

a logical network state entity coupled to the packing algorithm circuit and capable of being coupled to the packet source, the logical network state entity configured to communicate the actual traffic pattern to the source (Foster: see "as part of

registering…destination-side ports" in page 12, sections 0097 and 0098; see also "the network manager…with the configuration information" in page 13, section 104).

However, Foster does not explicitly disclose the following features:

receive the traffic pattern request from each of the plurality of packet sources in a predetermined time window,

wherein the actual traffic pattern comprises one of the plurality of first stage switches and one of the plurality of second stage switches such that the network is able to operate as a strictly non- interfering network.

Dell discloses a switch fabric for routing data between an input stage and an output stage comprising the feature:

receive the traffic pattern request from each of the plurality packet sources in a predetermined time window (Dell: see Figures 2, 3, and 12; see also "FIG.12 shows a block diagram…from other input devices" in page 8, sections 0111 - 0114).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Foster et al. using the feature, as taught by Dell, in order to provide a mechanism for receiving multiple requests/bids and resolving collisions among bids for the same output (Dell: see page 8, section 0110).

Furthermore, Karp discloses a multi-stage switching network for connecting any one of output ports to any one of input ports comprising the feature:

wherein the actual traffic pattern comprises one of the plurality of first stage switches and one of the plurality of second stage switches such that the network is able to operate as a strictly non-interfering network (Karp: see "Multi-stage switching…a single input port" in Abstract).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Foster et al. using the features, as taught by Karp, in order to provide a wide-sense non-blocking connecting path between input and output ports (Karp: see Abstract).

Regarding claim 2, *wherein the connection controller is configured to calculate a plurality of routing trees including the plurality of first stage and second stage switches* (Foster: see Figure 11 and "FIG. 11 is a flow diagram…next virtual identifier" in page 15, section 0114; ; see also "in some embodiment…destination node" in page 12, section 0097), *wherein the connection controller calculates a plurality of Destination Location Identifiers (DLIDs) and a set of forwarding instructions for each of the plurality of first stage and second stage switches, wherein the plurality of DLIDs correspond to one of the plurality of routing trees and one of a plurality of destinations in the network switches*

(Foster: see Figure 11 and "FIG. 11 is a flow diagram…next virtual identifier" in page 15, section 0114; ; see also "in some embodiment…destination node" in page 12, section 0097), *and wherein the connection controller populates a forwarding table of each of the plurality of first stage and second stage switches with the plurality of DLIDs and the set of forwarding instructions* (Foster: see "Each IFM may maintain…are to be forwarded" in page 6, section 0060).

Regarding claim 3, *wherein computing an actual traffic pattern comprises executing a rearrangement algorithm* (Foster: see Figure 7, 700; see also "The routine receives indications…appropriate information" in page 11, section 0093 and "as part of registering…appropriate destinations" in page 12, section 0097) *and assigning one of a plurality of Destination Location Identifiers (DLIDs) to the packet* (Foster: see Figure 7, 725, 73, 735, and 740; see also "If it is instead determined… translation table" in page 11, sections 0094 - 0095).

However, Foster et al. does not disclose the feature: *such that the network operates as a strictly non-interfering network*.

Karp discloses a multi-stage switching network for connecting any one of output ports to any one of input ports comprising the above feature (Karp: see "Multi-stage switching…a single input port" in Abstract).

Regarding claim 4, *wherein the packet follows a path through the one of the plurality of first stage switches and the one of the plurality of second stage switches,*

and wherein the one of the plurality of first stage switches and the one of the plurality of second stage switches forwards the packet according to the one of the plurality of DLIDs assigned to the packet (Foster: see Figure 7, 740 and "the routine continues to step 740…translation table" in page 11, section 0095; see also "When the source node…destination-side ports" in page 12, section 0098).

However, Foster et al. does not disclose the feature: *such that the network operates as a strictly non-interfering network*.

Karp discloses a multi-stage switching network for connecting any one of output ports to any one of input ports comprising the above feature (Karp: see "Multi-stage switching…a single input port" in Abstract).

Regarding claim 5, *wherein the one of the plurality of first stage switches and the one of the plurality of second stage switches each looks up the one of the plurality of DLIDs assigned to the packet in a forwarding table within the one of the plurality of first stage switches and the one of the plurality of second stage switches* (Foster: see Figure 7, 740 and "the routine continues to step 740…translation table" in page 11, section 0095; see also "When the source node…destination-side ports" in page 12, section 0098).

Regarding claim 6, *wherein the one of the plurality of first stage switches and the one of the plurality of second stage switches forwards the packet in accordance with the one of the plurality of DLIDs assigned to the packet as found in a forwarding table at*

each the portion of the plurality of switches (Foster: see Figure 7, 740 and "the routine continues to step 740…translation table" in page 11, section 0095).

Regarding claim 7, *wherein the network is a CLOS network* (Karp: see "Multi-stage switching…a single input port" in Abstract).

Regarding claim 8, *a connection controller* (Foster: see Figure 3, Network Manager, 370) *for a network comprising a plurality of first stage switches including a forwarding table* (Foster: see Figure 1, Interconnect Fabric 110 and "Each IFM may maintain…are to be forwarded" in page 6, section 0060), *a plurality of second stage switches including a forwarding table and coupled to each of the plurality of first stage switches* (Foster: see Figure 1, Interconnect Fabric 110 and "Each IFM may maintain…are to be forwarded" in page 6, section 0060), *and a plurality of nodes coupled the plurality of first stage switches* (Foster: see Figure 1, Node 1 through Node N, 105*), the connection controller comprising a computer-readable medium containing computer instructions for a processor that, when executed by the processor, cause the processor to perform a method* (Foster: see claim 59 in page 27) *comprising the steps of:*

calculating a plurality of routing trees, each routing tree comprising the plurality of first stage switches, and one of the plurality of second stage switches (Foster: see

Figure 11 and "FIG. 11 is a flow diagram…next virtual identifier" in page 15, section 0114),;

assigning a Destination Location Identifier (DLID) to each routing tree and to each node (Foster: see Figure 11 and "FIG. 11 is a flow diagram…next virtual identifier" in page 15, section 0114);

calculating a set of forwarding instructions for each of the plurality of first stage switches and each of the plurality of second stage switches based on the assigned DLIDs (Foster: see "Each IFM may maintain…are to be forwarded" in page 6, section 0060), *wherein the set of forwarding instructions causes the one of the plurality of first stage switches and the one of the plurality of second stage switches in each routing tree to operate in a manner that creates a path between each of the plurality of nodes* (Foster: see Figure 11 and "FIG. 11 is a flow diagram…next virtual identifier" in page 15, section 0114);

populating the forwarding table of each of the plurality of first stage switches and the plurality of second stage switches with the assigned DLIDs and the set of forwarding instructions (Foster: see "Each IFM may maintain…are to be forwarded" in page 6, section 0060; see also Figure 11 and "FIG. 11 is a flow diagram…next virtual identifier" in page 15, section 0114).

However, Foster does not explicitly disclose the following features:

computing and assigning a DLID to a packet to be transferred in the network based on all traffic pattern requests from the plurality of nodes in a predetermined time window such that the network operates as a strictly non-interfering network.

Dell discloses a switch fabric for routing data between an input stage and an output stage comprising the feature:

computing and assigning a DLID to a packet to be transferred in the network based on all traffic pattern requests from the plurality of nodes in a predetermined time window (Dell: see Figures 2, 3, and 12; see also "FIG.12 shows a block diagram…from other input devices" in page 8, sections 0111 - 0114).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Foster et al. using the feature, as taught by Dell, in order to provide a mechanism for receiving multiple requests/bids and resolving collisions among bids for the same output (Dell: see page 8, section 0110).

Furthermore, Karp discloses a multi-stage switching network for connecting any one of output ports to any one of input ports comprising the feature:

such that the network is able to operate as a strictly non-interfering network (Karp: see "Multi-stage switching…a single input port" in Abstract).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Foster et al. using the features, as taught by Karp, in order to provide a wide-sense non-blocking connecting path between input and output ports (Karp: see Abstract).

Regarding claim 9, *wherein the network is a CLOS network* (Karp: see "Multi-stage switching…a single input port" in Abstract).

Regarding claim 10, *wherein each of the plurality of nodes comprises a destination* (Foster: see Figure 2A 270, 275, and 280), *and wherein the destination is identified by a BaseLID* (Foster: see Figure 1, Node N+1, 105 and Figure 2B, column 213).

Regarding claim 13, *a computer-readable medium containing computer instructions for instructing a processor to perform a method for forwarding a packet from a source node of a plurality of nodes to a destination node of the plurality of nodes within a network comprising a plurality of first stage switches assigned a respective DLID, and a plurality of second stage switches coupled to each of the plurality of first*

stage switches and assigned a respective DLID, wherein a first switch of the plurality of first stage switches is further coupled to the source node and a second switch of the plurality of first stage switches is coupled to the destination node (Foster: see Figure 7), *the computer instructions, when executed by the processor, cause the processor to perform a method comprising the steps of:*

associating the destination node DLID with the packet (Foster: see "as part of registering…to each source node" in page 12, section 0097); *and*

routing the packet along a path through the first switch of the plurality of first stage switches, one of the plurality of second stage switches, and the second switch of the plurality of first stage switches to the destination based on the first switch DLID, the DLID of the one of the plurality of second stage switches, and the second switch DLID, wherein the first switch of the plurality of first stage switches, the one of the plurality of second stage switches, and the second switch of the plurality of first stage switches forward the packet according to the destination node DLID associated with the packet (Foster: see "Each IFM may maintain…are to be forwarded" in page 6, section 0060; see Figure 7, 740 and "the routine continues to step 740…translation table" in page 11, section 0095; see also "When the source node…destination-side ports" in page 12, section 0098).

However, Foster et al. does not disclose the feature:

computing and associating a destination node DLID with the packet based on the destination node and all traffic pattern requests from the plurality of nodes in a

predetermined time window such that the network operates as a strictly non-interfering network.

Dell discloses a switch fabric for routing data between an input stage and an output stage comprising the feature:

computing and associating a destination node DLID with the packet based on the destination node and all traffic pattern requests from the plurality of nodes in a predetermined time window (Dell: see Figures 2, 3, and 12; see also "FIG.12 shows a block diagram…from other input devices" in page 8, sections 0111 - 0114).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Foster et al. using the feature, as taught by Dell, in order to provide a mechanism for receiving multiple requests/bids and resolving collisions among bids for the same output (Dell: see page 8, section 0110).

Karp discloses a multi-stage switching network for connecting any one of output ports to any one of input ports comprising the above feature:

such that the network operates as a strictly non-interfering network (Karp: see "Multi-stage switching…a single input port" in Abstract).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Foster et al. using the features, as taught by Karp, in order to provide a wide-sense non-blocking connecting path between input and output ports (Karp: see Abstract).

Regarding claim 15, *wherein the network is a CLOS network* (Karp: see "Multi-stage switching…a single input port" in Abstract).

Regarding claim 16, *wherein routing the packet comprises looking up the destination node DLID associated with the packet in a forwarding table within each of the first switch of the plurality of first stage switches, the one of the plurality of second stage switches, and the second switch of the plurality of first stage switches along the path from the source node to the destination node* (Foster: see "Each IFM may maintain…are to be forwarded" in page 6, section 0060; see Figure 7, 740 and "the routine continues to step 740…translation table" in page 11, section 0095; see also "When the source node…destination-side ports" in page 12, section 0098).

Regarding claim 17, *wherein routing step comprises the step of routing the packet in accordance with the destination node DLID associated with the packet as found in a forwarding table included within each of the first switch of the plurality of first*

stage switches, the one of the plurality of second stage switches, and the second switch of the plurality of first stage switches (Foster: see "Each IFM may maintain…are to be forwarded" in page 6, section 0060; see Figure 7, 740 and "the routine continues to step 740…translation table" in page 11, section 0095; see also "When the source node…destination-side ports" in page 12, section 0098).

Regarding claim 21, *further comprising instructions that, when executed by the processor, cause the processor to further perform the steps of:*

recognizing if a new node, a new switch, or both is added to the network (Foster: see "the network manager identifies paths...from a source node" in page 12, section 0100; see also "the network manager…directly connected" in page 12, section 0102); *and*

executing a rearrangement algorithm for the network in response to recognizing the new node, the new switch, or both (Foster: see "the network manager identifies paths...from a source node" in page 12, section 0100; "the network manager…directly connected" in page 12, section 0102; see also Figures 8 and 9; see also "the network manager may dynamically discover...to another device" in page 13, sections 0110 - 0111).

3. Claims 11-12, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster et al. (US 2002/0181395 A1) in view of Dell et al. (US

2002/0085578 A1) and Karp (5,469,154), and further in view of Brahmaroutu (US 2003/0033427 A1).

Foster et al. and Karp disclose all the limitations as in paragraph 2 above. Foster et al. and Karp do not explicitly disclose the following features: regarding claim 11, *wherein each of the plurality of second stage switches comprises a spine node, and wherein calculating the plurality of routing trees comprises, for each spine node in the network, calculating a shortest path from each spine node to each of the plurality of end nodes; r*egarding claim 12, *wherein each of the plurality of second stage switches comprises a spine node, and wherein each of the plurality of routing trees further comprises a plurality of links that form a shortest path from each end node to each spine node*; regarding claim 18, *wherein each of the plurality of first stage switches is an INFINIBAND switch and each of the plurality of second stage switches is an INFINIBAND switch*; regarding claim 19, *wherein each of the plurality of first stage switches is an INFINIBAND switch and each of the plurality of second stage switches is an INFINIBAND switch*; regarding claim 20, *wherein each of the plurality of first stage switches is an 1NFINIBAND switch and each of the plurality of second stage switches is an INFINIBAND switch.*

Brahmaroutu discloses a mechanism to program forwarding tables comprising the following features:

Regarding claim 11, *wherein each of the plurality of second stage switches comprises a spine node* (Brahmaroutu: see Figure 4), *and wherein calculating the plurality of routing trees comprises, for each spine node in the network, calculating a shortest path from each spine node to each of the plurality of end nodes* (Brahmaroutu: see Figure 6 and "FIG. 6 illustrates…recorded in TABLE 1" in page 5, sections 0040 – 0042; see also "TABLE 2 shows…the destination switch" in page 6, section 0047).

Regarding claim 12, *wherein each of the plurality of second stage switches comprises a spine node* (Brahmaroutu: see Figure 4), *and wherein each of the plurality of routing trees further comprises a plurality of links that form a shortest path from each end node to each spine node* (Brahmaroutu: see Figure 6 and "FIG. 6 illustrates…recorded in TABLE 1" in page 5, sections 0040 – 0042; see also "TABLE 2 shows…the destination switch" in page 6, section 0047).

Regarding claim 18, *wherein each of the plurality of first stage switches is an INFINIBAND switch and each of the plurality of second stage switches is an INFINIBAND switch* (Brahmaroutu: see "According to…by the InfiniBand™ Trade Association" in page 2, section 0021).

Regarding claim 19, *wherein each of the plurality of first stage switches is an INFINIBAND switch and each of the plurality of second stage switches is an*

INFINIBAND switch (Brahmaroutu: see "According to…by the InfiniBand™ Trade Association" in page 2, section 0021).

Regarding claim 20, *wherein each of the plurality of first stage switches is an 1NFINIBAND switch and each of the plurality of second stage switches is an INFINIBAND switch* (Brahmaroutu: see "According to…by the InfiniBand™ Trade Association" in page 2, section 0021).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Karp with Foster et al. using the features, as taught by Brahmaroutu, in order to program switch forwarding tables without any routing ambiguity (Brahmaroutu: see "The subnet manager…between switches" in page 6, section 0059).

Response to Arguments

4. Applicant's arguments with respect to claims 1, 8, and 13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUVENA LOO whose telephone number is (571)270-1974. The examiner can normally be reached on Monday - Friday: 7:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JUVENA LOO/
Examiner
Art Unit 2416
October 7, 2008

/Kwang B. Yao/
Supervisory Patent Examiner, Art Unit 2416